

This listing of claims will replace all prior versions,  
and listings, of claims in the application:

1 Claim 1 (currently amended): A solid-state imaging device  
2 comprising:  
3 a pixel unit constituted by a two-dimensional array of  
4 pixels for generating charge in correspondence to received  
5 light and accumulating the charge for a predetermined  
6 period of time;  
7 a vertical transfer unit for vertically transferring  
8 charge from the pixels in the pixel unit, a horizontal  
9 transfer unit for horizontally transferring charge from the  
10 vertical transfer unit;  
11 shift gates each provided between each pixel and the  
12 vertical transfer unit for reading out the charge in the  
13 pixels to the vertical transfer unit, gate electrodes for  
14 controlling the shift gates; and  
15 a plurality of lead lines for connecting the gate  
16 electrodes to an external circuit and a plurality of  
17 connection terminals for connecting the gate electrodes to  
18 the external circuit,  
19 the gate electrodes making up N of gate electrode  
20 groups in which the lines belonging to each coset of modulo  
21 N within successive pixel rows are connected to common lead  
22 lines, N being a predetermined natural number between 4 and  
23 one half the number of pixels in a column, and N also being  
24 the minimum periodic unit of connections from said gate  
25 electrodes having the same modulo N value and belonging to  
26 different gate electrode groups to said connection  
27 terminals within said successive pixel rows, the gate  
28 ~~electrodes~~ electrode groups having common connection  
29 terminals to

30 (i) reduce the number of the connection terminals to  
31 less than N, and  
32 (ii) enable the gate electrodes having common  
33 connection terminals to be controlled with different  
34 timing from the timing of non-common connection  
35 terminals of the gate electrode groups.

1 Claim 2 (currently amended): A solid-state imaging device  
2 comprising:  
3 a pixel unit constituted by a two-dimensional array of  
4 pixels for generating charge in correspondence to received  
5 light and accumulating the charge for a predetermined  
6 period of time;  
7 a vertical transfer unit for vertically transferring  
8 charge from the pixels in the pixel unit, a horizontal  
9 transfer unit for horizontally transferring charge from the  
10 vertical transfer unit;  
11 shift gates each provided between each pixel and the  
12 vertical transfer unit for reading out the charge in the  
13 pixels to the vertical transfer unit, gate electrodes for  
14 controlling the shift gates; and  
15 a plurality of lead lines for connecting the gate  
16 electrodes to an external circuit and a plurality of  
17 connection terminals for connecting the gate electrodes to  
18 the external circuit,  
19 gate control lines connected to gate electrode groups  
20 in which horizontal lines belonging to each coset of modulo  
21 N within successive pixel rows are connected commonly, N  
22 being a predetermined natural number between 4 and one half  
23 the number of pixels in a column, and N also being the  
24 minimum periodic unit of connections from said gate  
25 electrodes having the same modulo N value and belonging to

26 different gate electrode groups to said connection  
27 terminals within said successive pixel rows, being combined  
28 with each other so as to  
29 (i) reduce the number of the connection terminals to  
30 less than N, and  
31 (ii) enable the gate electrodes having common  
32 connection terminals to be controlled with different  
33 timing from the timing of non-common connection  
34 terminals of the gate electrode groups.

1 Claim 3 (currently amended): A solid-state imaging device  
2 comprising:  
3 a pixel unit constituted by a two-dimensional array of  
4 pixels for generating charge in correspondence to received  
5 light and accumulating the charge for a predetermined  
6 period of time;  
7 a vertical transfer unit for vertically transferring  
8 charge from the pixels in the pixel unit, a horizontal  
9 transfer unit for horizontally transferring charge from the  
10 vertical transfer unit;  
11 shift gates each provided between each pixel and the  
12 vertical transfer unit for reading out the charge in the  
13 pixels to the vertical transfer unit, gate electrodes for  
14 controlling the shift gates; and  
15 a plurality of lead lines for connecting the gate  
16 electrodes to an external circuit and a plurality of  
17 connection terminals for connecting the gate electrodes to  
18 the external circuit,  
19 the gate electrodes being provided in a predetermined  
20 number N of gate electrode groups such that horizontal line  
21 number of the gate electrode groups which are connected to  
22 respective common lead lines belong to each same residue

23 class of modulo N, N being a predetermined natural number  
24 between 4 and one half the number of pixels in a column,  
25 and N also being the minimum periodic unit of connections  
26 from said gate electrodes having the same modulo N value  
27 and belonging to different gate electrode groups to said  
28 connection terminals within said successive pixel rows,  
29 some of the gate electrode groups being commonly connected  
30 (i) so that the connection terminals are less in  
31 number than N, and  
32 (ii) to enable the gate electrodes having common  
33 connection terminals to be controlled with different  
34 timing from the timing of non-common connection  
35 terminals of the gate electrode groups.

1 Claim 4 (currently amended): A solid-state imaging device  
2 comprising:  
3 a pixel unit constituted by a two-dimensional array of  
4 pixels for generating charge in correspondence to received  
5 light and accumulating the charge for a predetermined  
6 period of time;  
7 a vertical transfer unit for vertically transferring  
8 charge from the pixels in the pixel unit, a horizontal  
9 transfer unit for horizontally transferring charge from the  
10 vertical transfer unit;  
11 shift gates each provided between each pixel and the  
12 vertical transfer unit for reading out the charge in the  
13 pixels to the vertical transfer unit, gate electrodes for  
14 controlling the shift gates; and  
15 a plurality of lead lines for connecting the gate  
16 electrodes to an external circuit and a plurality of  
17 connection terminals for connecting the gate electrodes to  
18 the external circuit,

19 the gate electrodes making up N of gate electrode  
20 groups in which the lines belonging to each coset of modulo  
21 N within successive pixel rows are connected to common lead  
22 lines, N being a predetermined natural number between 4 and  
23 one half the number of pixels in a column, and N also being  
24 the minimum periodic unit of connections from said gate  
25 electrodes having the same modulo N value and belonging to  
26 different gate electrode groups to said connection  
27 terminals within said successive pixel rows, the gate  
28 electrode groups having common connections to  
29 (i) reduce the number of the connection terminals to  
30 less than N, and  
31 (ii) enable the gate electrodes having common  
32 connection terminals to be controlled with different  
33 timing from the timing of non-common connection  
34 terminals of the gate electrode groups,  
35 wherein the commonly connected gate electrode groups  
36 are always controlled in the same way in each of all  
37 predetermined read-out modes including selective pixel  
38 read-out modes by selective shift gate driving.

1 Claim 5 (currently amended): A solid-state imaging device  
2 comprising:  
3 a pixel unit constituted by a two-dimensional array of  
4 pixels for generating charge in correspondence to received  
5 light and accumulating the charge for a predetermined  
6 period of time;  
7 a vertical transfer unit for vertically transferring  
8 charge from the pixels in the pixel unit, a horizontal  
9 transfer unit for horizontally transferring charge from the  
10 vertical transfer unit;

11 shift gates each provided between each pixel and the  
12 vertical transfer unit for reading out the charge in the  
13 pixels to the vertical transfer unit, gate electrodes for  
14 controlling the shift gates; and

15 a plurality of lead lines for connecting the gate  
16 electrodes to an external circuit and a plurality of  
17 connection terminals for connecting the gate electrodes to  
18 the external circuit,

19 gate control lines connected to gate electrode groups  
20 in which the horizontal lines belonging to each coset of  
21 modulo  $N$  within successive pixel rows are connected  
22 commonly,  $N$  being a predetermined natural number between 4  
23 and one half the number of pixels in a column, and  $N$  also  
24 being the minimum periodic unit of connections from said  
25 gate electrodes having the same modulo  $N$  value and  
26 belonging to different gate electrode groups to said  
27 connection terminals within said successive pixel rows,  
28 being combined with each other so as to

29 (i) reduce the number of the connection terminals to  
30 less than  $N$ , and

31 (ii) enable the gate electrodes having common  
32 connection terminals to be controlled with different  
33 timing from the timing of non-common connection  
34 terminals of the gate electrode groups,

35 wherein the commonly connected gate electrode groups  
36 are always controlled in the same way in each of all  
37 predetermined read-out modes including selective pixel  
38 read-out modes by selective shift gate driving.

1 Claim 6 (currently amended): A solid-state imaging device  
2 comprising:

3 a pixel unit constituted by a two-dimensional array of  
4 pixels for generating charge in correspondence to received  
5 light and accumulating the charge for a predetermined  
6 period of time;

7 a vertical transfer unit for vertically transferring  
8 charge from the pixels in the pixel unit, a horizontal  
9 transfer unit for horizontally transferring charge from the  
10 vertical transfer unit;

11 shift gates each provided between each pixel and the  
12 vertical transfer unit for reading out the charge in the  
13 pixels to the vertical transfer unit, gate electrodes for  
14 controlling the shift gates; and

15 a plurality of lead lines for connecting the gate  
16 electrodes to an external circuit and a plurality of  
17 connection terminals for connecting the gate electrodes to  
18 the external circuit,

19 the gate electrodes being provided in a predetermined  
20 number  $N$  of gate electrode groups such that horizontal line  
21 number of the gate electrode groups which are connected to  
22 respective common lead lines belong to each same residue  
23 class of modulo  $N$ ,  $N$  being a predetermined natural number  
24 between 4 and one half the number of pixels in a column,  
25 and  $N$  also being the minimum periodic unit of connections  
26 from said gate electrodes having the same modulo  $N$  value  
27 and belonging to different gate electrode groups to said  
28 connection terminals within said successive pixel rows,  
29 some of the gate electrode groups being commonly connected

30 (i) so that the connection terminals are less in  
31 number than  $N$ , and

32 (ii) to enable the gate electrodes having common  
33 connection terminals to be controlled with different

34 timing from the timing of non-common connection  
35 terminals of the gate electrode groups,  
36 wherein the commonly connected gate electrode groups  
37 are always controlled in the same way in each of all  
38 predetermined read-out modes including selective pixel  
39 read-out modes by selective shift gate driving.

1 Claim 7 (previously presented): The solid-state imaging  
2 device according to claim 4, wherein gate electrode groups  
3 controlled in each of all the predetermined read-out modes  
4 are set such as to provide a minimum number of connection  
5 terminals for connecting the gate electrodes to an external  
6 circuit.

1 Claim 8 (previously presented): The solid-state imaging  
2 device according to claim 5 wherein gate electrode groups  
3 controlled in each of all the predetermined read-out modes  
4 are set such as to provide a minimum number of connection  
5 terminals for connecting the gate electrodes to an external  
6 circuit.

1 Claim 9 (previously presented): The solid-state imaging  
2 device according to claim 6 wherein gate electrode groups  
3 controlled in each of all the predetermined read-out modes  
4 are set such as to provide a minimum number of connection  
5 terminals for connecting the gate electrodes to an external  
6 circuit.

Claims 10 and 11 (canceled)

1 Claim 12 (previously presented): The solid-state imaging  
2 device of claim 1 wherein at least two horizontal lines



3 belonging to the same pixel group but to different gate  
4 electrode groups are connected to a common connection  
5 terminal.

1 Claim 13 (previously presented): The solid-state imaging  
2 device of claim 2 wherein at least two horizontal lines  
3 belonging to the same pixel group but to different gate  
4 electrode groups are connected to a common connection  
5 terminal.

1 Claim 14 (previously presented): The solid-state imaging  
2 device of claim 3 wherein at least two horizontal lines  
3 belonging to the same pixel group but to different gate  
4 electrode groups are connected to a common connection  
5 terminal.

1 Claim 15 (previously presented): The solid-state imaging  
2 device of claim 4 wherein at least two horizontal lines  
3 belonging to the same pixel group but to different gate  
4 electrode groups are connected to a common connection  
5 terminal.

1 Claim 16 (previously presented): The solid-state imaging  
2 device of claim 5 wherein at least two horizontal lines  
3 belonging to the same pixel group but to different gate  
4 electrode groups are connected to a common connection  
5 terminal.

1 Claim 17 (previously presented): The solid-state imaging  
2 device of claim 6 wherein at least two horizontal lines  
3 belonging to the same pixel group but to different gate  
4 electrode groups are connected to a common connection  
5 terminal.

1 Claim 18 (previously presented): The solid-state imaging  
2 device of claim 1 wherein only two connection terminals  
3 connected to said vertical transfer unit are not connected  
4 to any of the gate electrodes.

1 Claim 19 (previously presented): The solid-state imaging  
2 device of claim 2 wherein only two connection terminals  
3 connected to said vertical transfer unit are not connected  
4 to any of the gate electrodes.

1 Claim 20 (previously presented): The solid-state imaging  
2 device of claim 3 wherein only two connection terminals  
3 connected to said vertical transfer unit are not connected  
4 to any of the gate electrodes.

1 Claim 21 (previously presented): The solid-state imaging  
2 device of claim 4 wherein only two connection terminals  
3 connected to said vertical transfer unit are not connected  
4 to any of the gate electrodes.

1 Claim 22 (previously presented): The solid-state imaging  
2 device of claim 5 wherein only two connection terminals  
3 connected to said vertical transfer unit are not connected  
4 to any of the gate electrodes.

1 Claim 23 (previously presented): The solid-state imaging  
2 device of claim 6 wherein only two connection terminals  
3 connected to said vertical transfer unit are not connected  
4 to any of the gate electrodes.

1 Claim 24 (previously presented): The solid-state imaging  
2 device of claim 1 wherein connections from said gate

3 electrodes to said connection terminals within successive  
4 pixel rows have a periodic repetition, and wherein N is the  
5 minimum period of repetition.

1 Claim 25 (previously presented): The solid-state imaging  
2 device of claim 1 wherein connections from said gate  
3 electrodes to said connection terminals within successive  
4 pixel rows exhibit a repeating pattern, and wherein N is  
5 the minimum period of the repeating pattern.